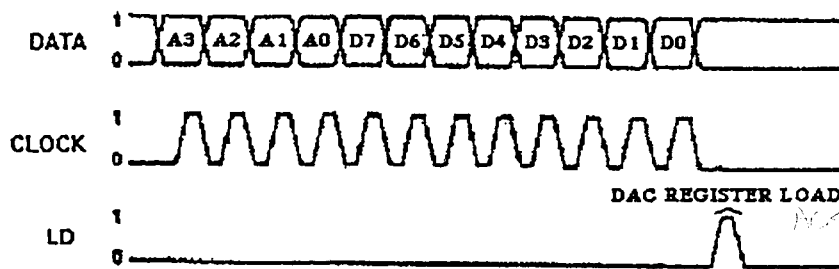


2.2 The DAC bus *Electrical Definition Control*

The DAC bus consists of two HCMOS signals, DATA and CLOCK, which are output on backplane connector P1. In association with the I²C bus, these signals allow the CLM to load values into digital-to-analog converters (DACs) on other modules in the projector. Currently, the only type of device attached to the DAC bus is the Analog Devices DAC-8840, an octal 8-bit multiplying DAC. Data is loaded into this device by sequencing a 12-bit word on the DATA line. Each bit of data is clocked in with a low-to-high transition on the CLOCK line. The 12-bit word consists of a 4-bit address (A0-A3) to select the DAC channel, followed by an 8-bit data word (D0-D7). When all 12 bits have been clocked in, an active high strobe on the chip's LD (load) input writes the data into the selected channel. The LD pulse comes from an output of an I²C I/O port (PCF8574A) on the same module as the DAC. The output is toggled by software to create the LD pulse. When multiple DACs exist on the same module, each receives its own dedicated LD pulse.

The timing of a data transfer cycle is illustrated below. The clock rate is software dependent.



2.3 The Parallel Bus

The parallel bus is used to control optional cards inserted into the ACON and "spare" slots of the projector. The bus signals, which appear on backplane connector P1, originate from the 68000 microprocessor used in the CPU (see section 3.0 'Circuit Description'). The bus consists of address lines (A1-A16), data lines (D0-D15), bus control lines (RW, UDS*, LDS*, CS-ACON*, and CS-SPARE*), and other signals (ACON-RD, ACON-WR, ACON-I and RESET*). All signals are buffered HCMOS. When the cards are not being addressed, the address lines, data lines and bus control signals are inactive and are pulled either HIGH or LOW.

RW (read/write) is LOW during write cycles. LDS* (lower data strobe) is LOW when data is transferred on D0-D7. UDS* is LOW when data is transferred on D8-D15. Both LDS* and UDS* are LOW when 16-bit words are transferred on the bus. CS-ACON* and CS-SPARE* are active LOW chip selects for the ACON slot and "spare" slot, respectively.

ACON-RD, ACON-WR, ACON-I and RESET* support communication with a coprocessor on the ACON card. ACON-RD goes HIGH when the coprocessor reads data from the 68000. ACON-WR goes HIGH when the coprocessor writes data to the 68000. ACON-I goes high when either action occurs. RESET* goes LOW when the 68000 microprocessor is reset, serving to initialize the communication hardware on the ACON card.